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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Schloesser, *et al.* Docket No.: INF-135
Serial No.: 10/777,128 Art Unit: 2818
Patent No.: 7,109,544 B2 Issue Date: September 19, 2006
Filed: February 13, 2004 Examiner: Andy Huynh
For: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Request for Issuance of Certificate of Correction
Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322

Dear Sir:

Upon review of the above-identified issued patent, Patentee notes errors in the patent that should be corrected as shown on the attached Certificate of Correction.

The mistakes noted on the attached Certificate of Correction were incurred through the fault of the Patent and Trademark Office. Accordingly, no fee is required.

Patentee respectfully solicits the issuance of the requested Certificate of Correction.

Respectfully submitted,

Ira S. Matsil
Attorney for Patentee
Reg. No. 35,272

10/24/06

Date

SLATER & MATSIL, L.L.P.
17950 Preston Rd.
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Certificate
NOV 02 2006
of Correction

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. 7,109,544 B2
APPLICATION NO. : 10/777,128
ISSUE DATE : September 19, 2006
INVENTOR(S) : Schloesser, *et al.*

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the References Cited Field (56) on the coversheet, line 14, delete "2002/0109178" insert --2002/0109176--
In the Abstract Field (57) on the coversheet, line 1, delete "substrate vertical" insert --substrate, vertical--
In the Abstract Field (57) on the coversheet, line 6, delete "connection for" insert --connection, for--
Column 8, line 15; delete "521" insert --52--
Column 16, line 2; delete "fanned" insert --formed--
Column 16, line 52; delete "Wenches" insert --Trenches--
Column 17, line 13; delete "raw" insert --row--

MAILING ADDRESS OF SENDER(Please do not use customer number below):

Slater & Matsil, L.L.P.
17950 Preston Road, Suite 1000
Dallas, Texas 75252

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application for to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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For: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit: October 24, 2006

I hereby certify that the below listed correspondence is being deposited with the United States Postal Service on the date indicated above as first class mail in an envelope addressed to: Certificate of Corrections Branch, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

Certificate of Mailing via First Class Mail (1 page)
Request for Issuance of Certificate of Correction (1 page)
Certificate of Correction (1 original and 1 copy)
Return Postcard

Respectfully submitted,

Michelle Reyes
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